Lithography Options for Future Logic ICs

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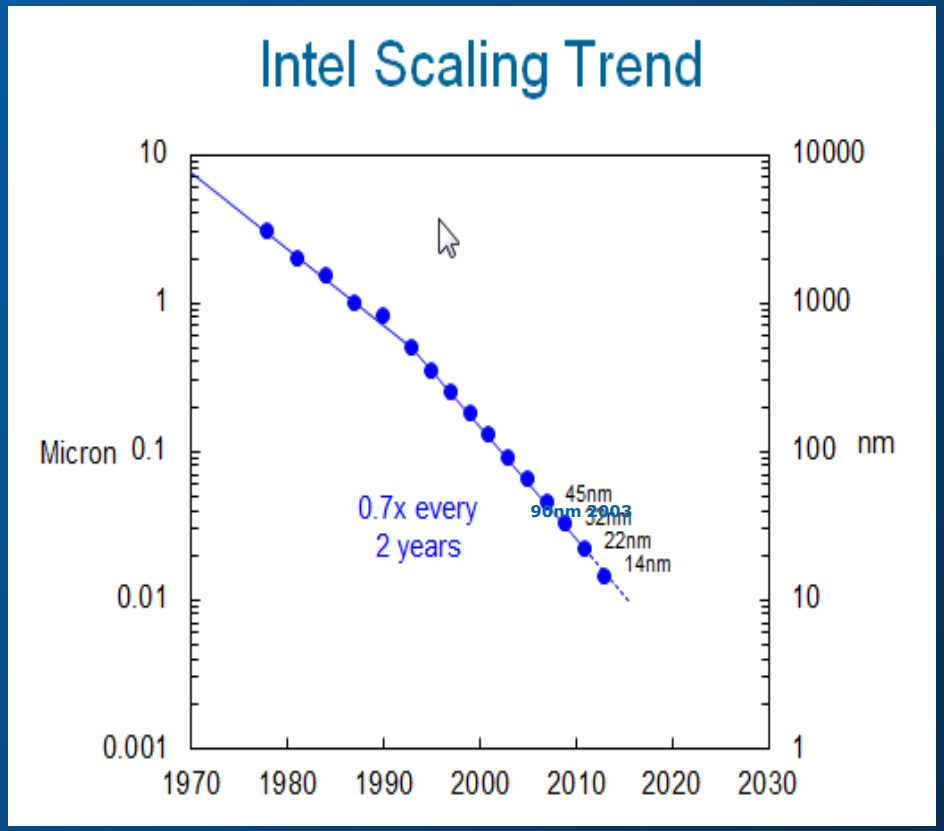
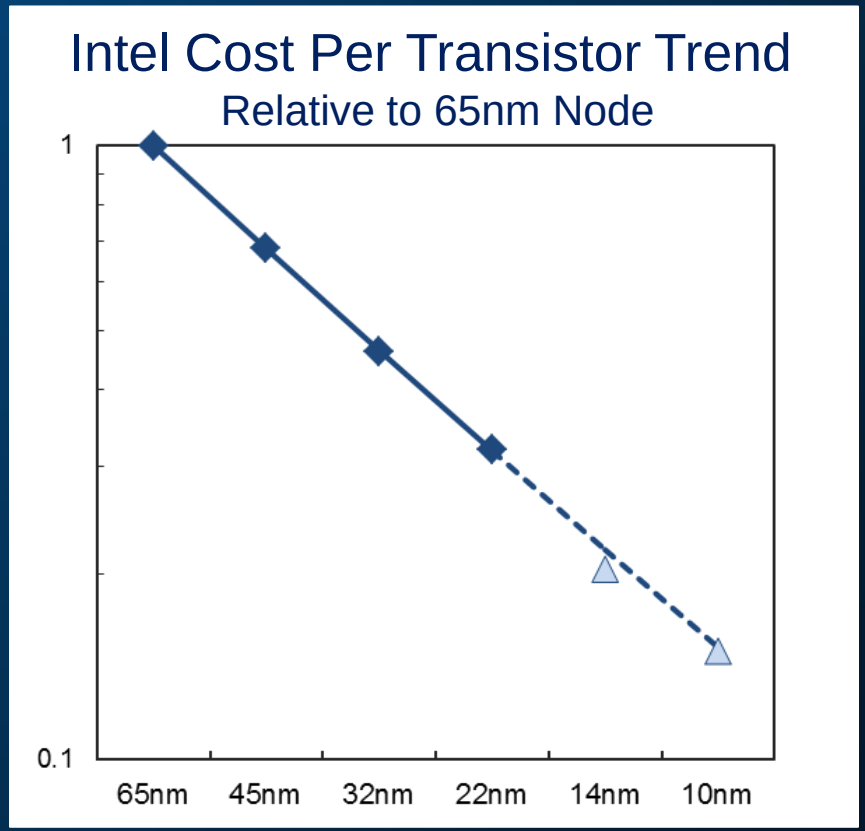
Intel Corporation

“No physical quantity can continue to change exponentially forever. Your job is delaying forever”

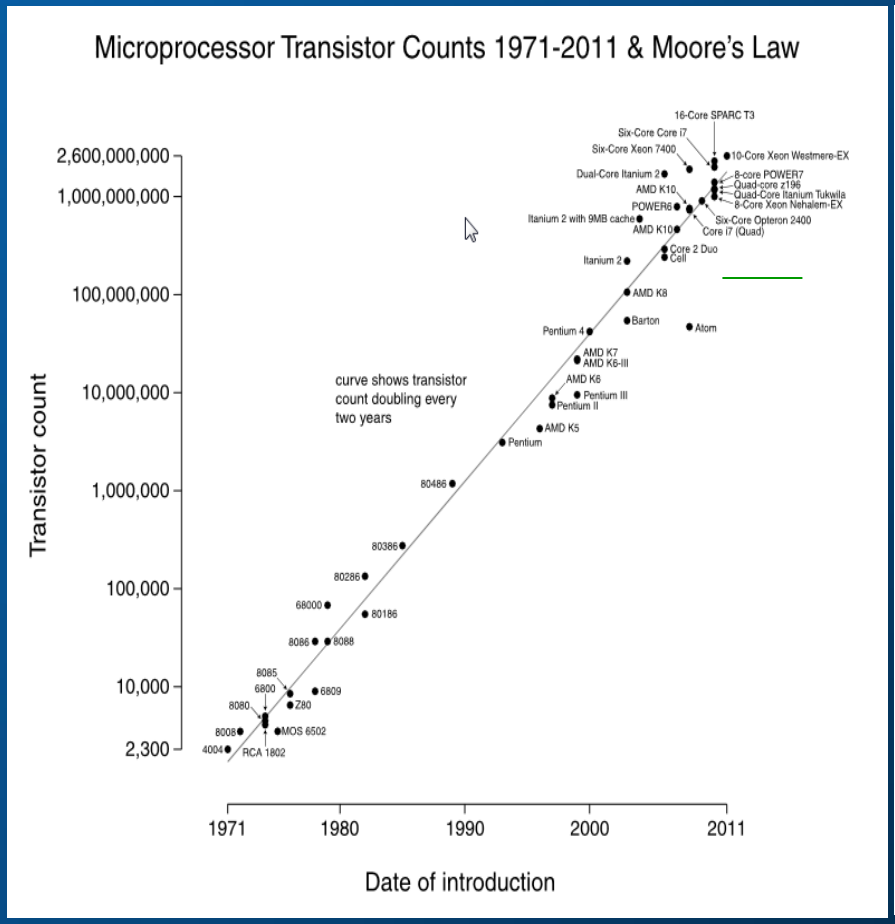
Gordon Moore, ISSCC 2003 Keynote



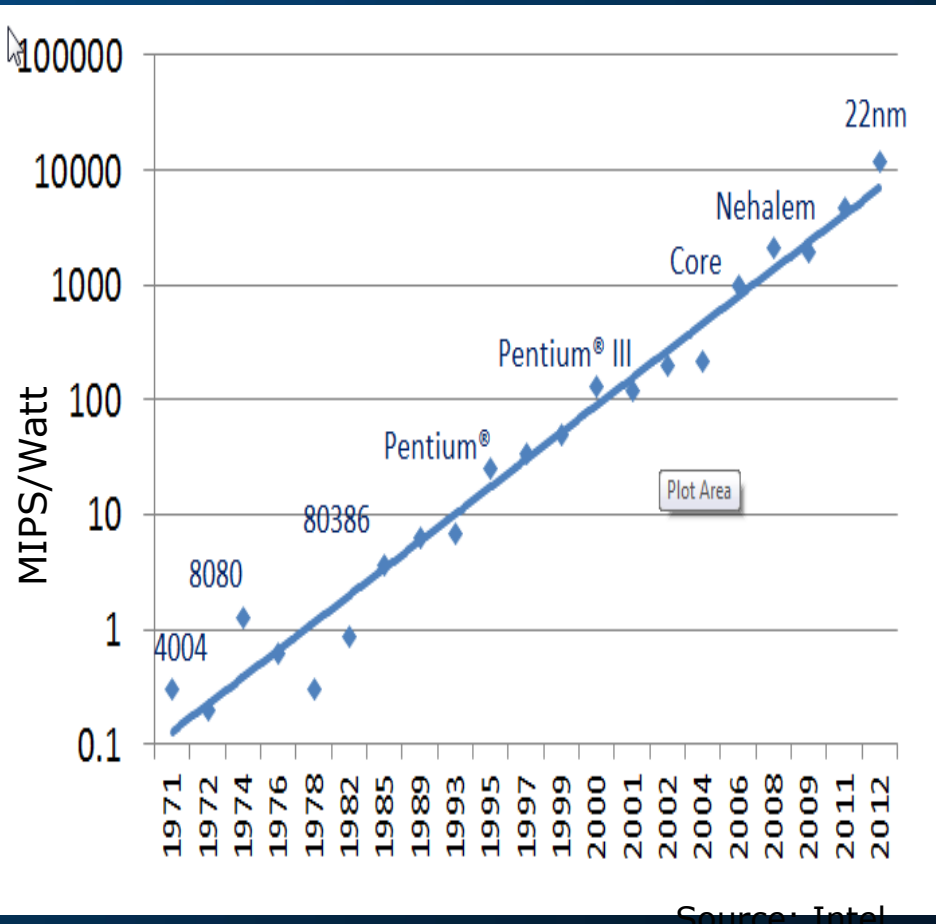


We did as expected in 10 years following Gordon’s Talk

Moore's Law



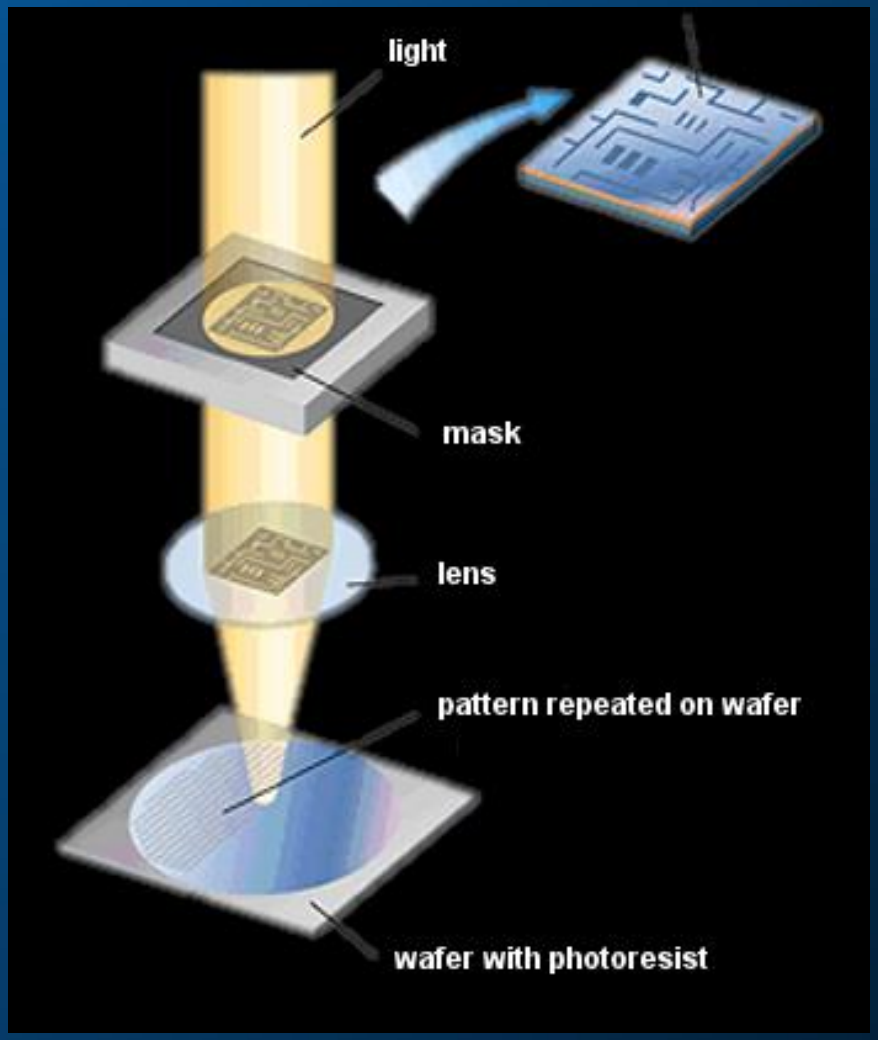
Koomey's Law



Source: Intel

Growth in transistor count and process innovation led to new products and better computational efficiency

Lithography is a Process that Transfers Circuit Design Intent onto the Wafer

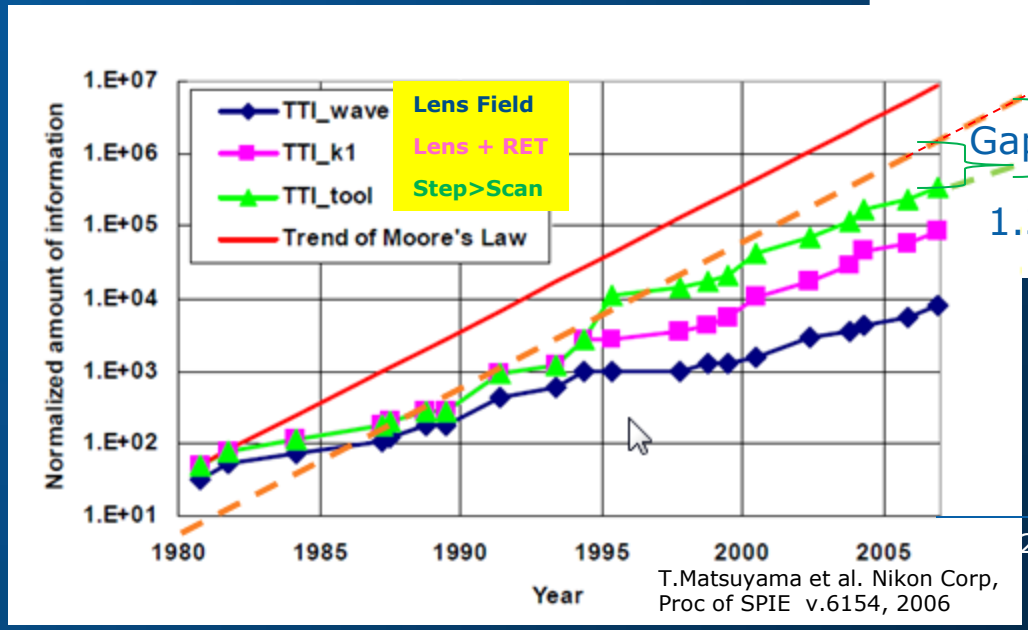


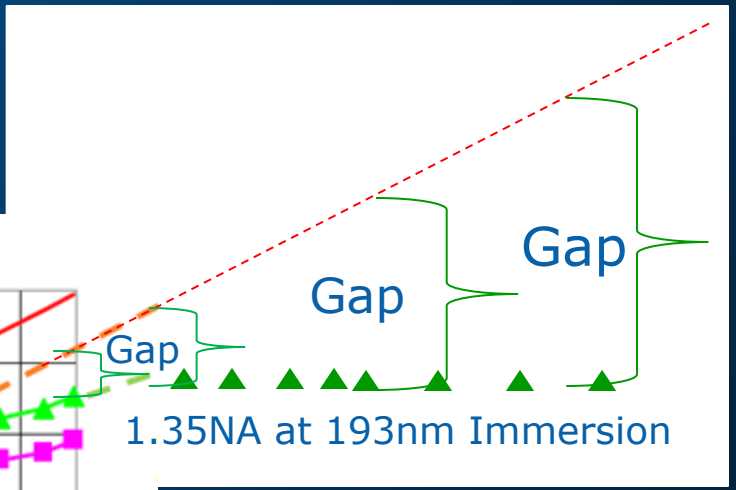
Information:

Channel Capacity
Channel Loss
Channel Rate
Transfer Cost

Single Exposure Channel Information Capacity Gap

1.35NA 193nm Scanner is "End of the Road" DUV Lithography Tool

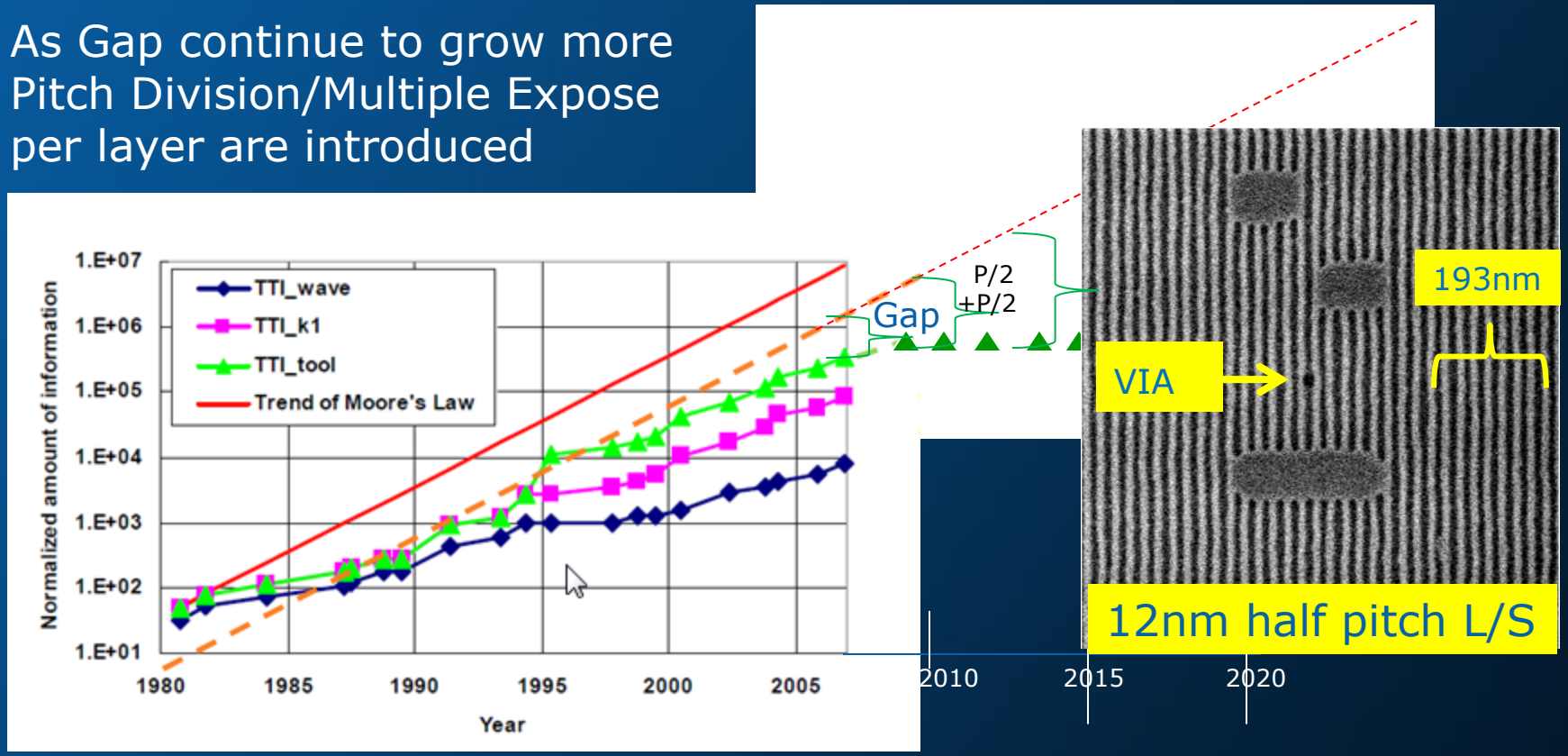




Gap between Scanner Information Transfer Capacity and IC need resulted in Pitch Division introduction in HVM for 22nm MPU Products.

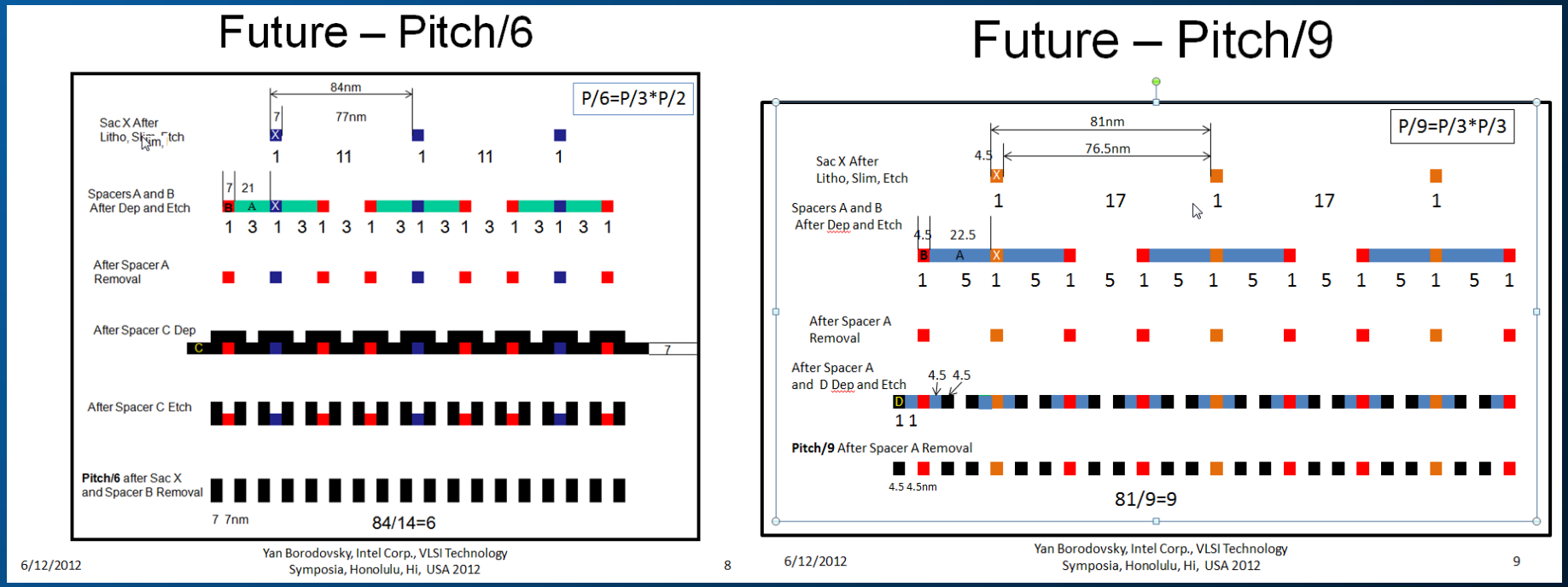
Multiple Exposures Needed to Close the Gap

As Gap continue to grow more Pitch Division/Multiple Expose per layer are introduced



Pitch Division and Multiple Exposures per Layer work for Density Scaling far below Single Expose limits

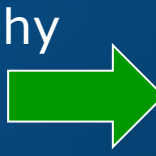
Multiple Exposures Needed to Close the Gap

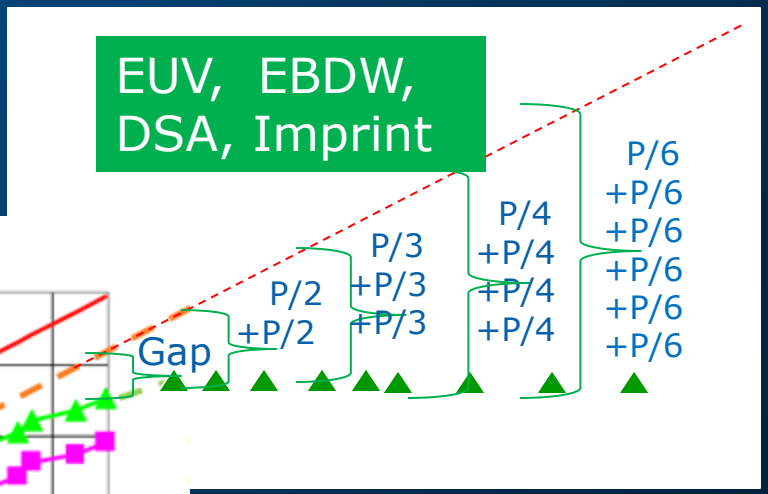


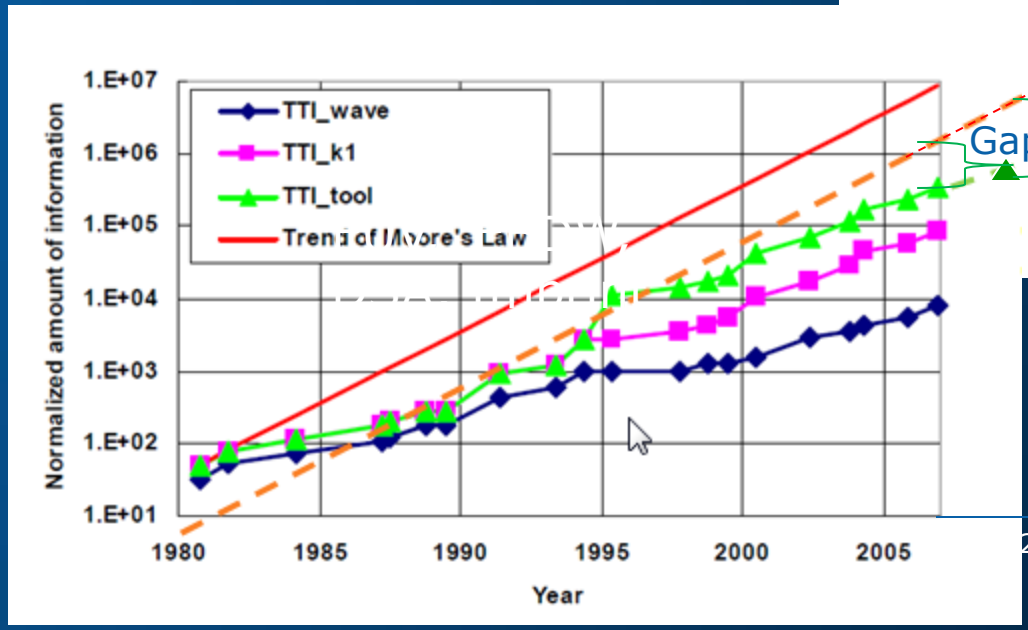
Solutions to Extend Pitch Division Suggested

Multiple Exposures Needed to Close the Gap

Next Generation Lithography (NGL) Contenders



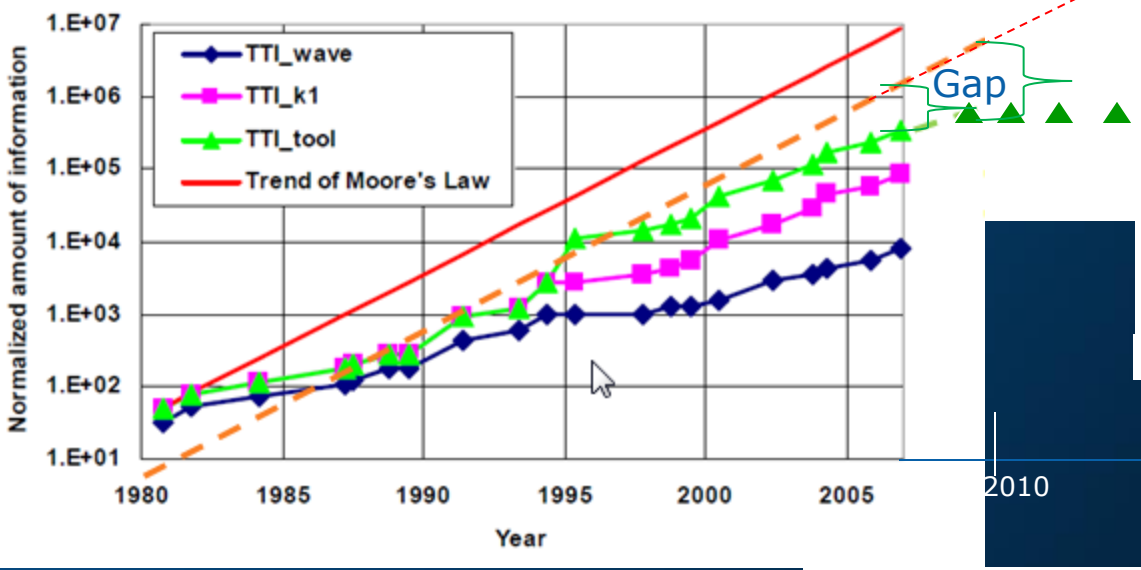


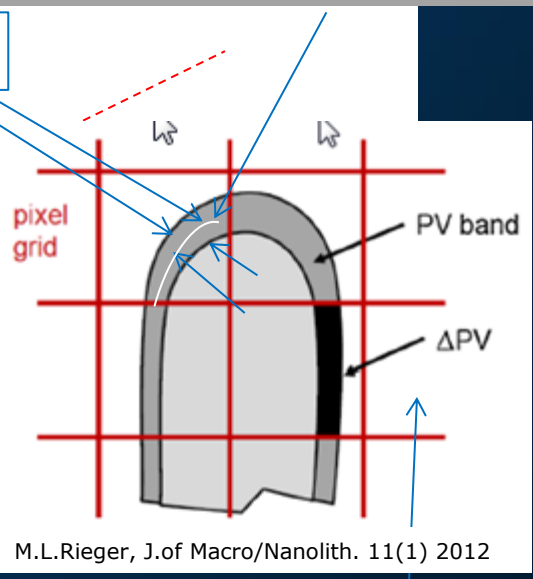


So, why Worldwide efforts to abandon Pattern Split/Multiple Expose?

Single Exposure/Channel Information Capacity

Controlling Edge Placement Errors (EPE) becomes more and more difficult with multiple pattern splits





$$\text{capacity}_{\frac{\text{bits}}{\text{area}}} = \left(\frac{\text{pixels}}{\text{area}}\right) \cdot \left(\frac{\text{bits}}{\text{pixel}}\right)$$

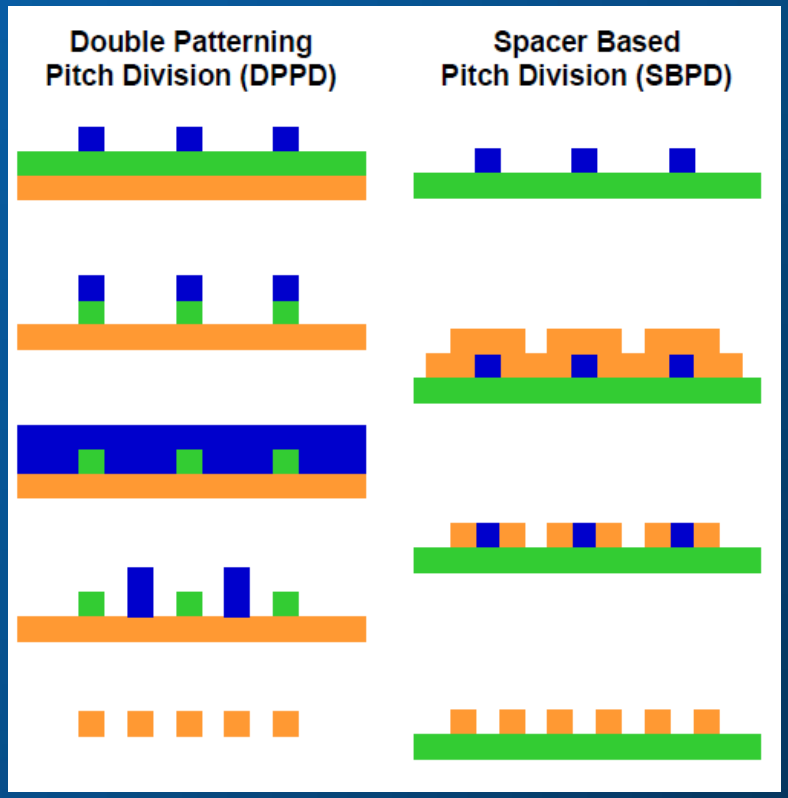
$$= 4\text{BW}_x\text{BW}_y \cdot \left[\frac{1}{2}\log_2\left(1+\frac{s}{n}\right)\right].$$

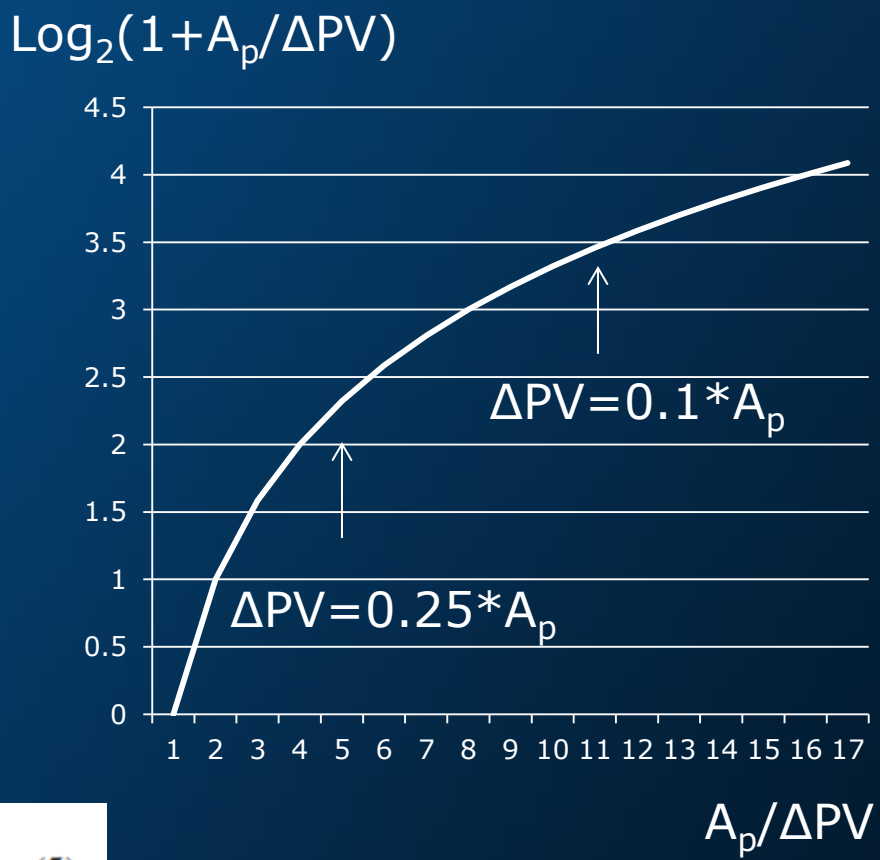
$$\frac{\text{bits}}{\text{pixel}} = \log_2\left(1+\frac{A_p}{\Delta\text{PV}}\right). \quad (5)$$

Mike Rieger proposed Lithographer friendly treatment of assessing s/n

$$\frac{\text{bits}}{m^2} = \left[\frac{\text{NA}}{k_1\lambda}\right]^2 \log_2(M_H) = \left[\frac{\text{NA}}{k_1\lambda}\right]^2 \log_2\left(1+\frac{A_p}{\Delta\text{PV}}\right). \quad (6)$$

Cumulative Information Capacity of Split/Divided Exposures





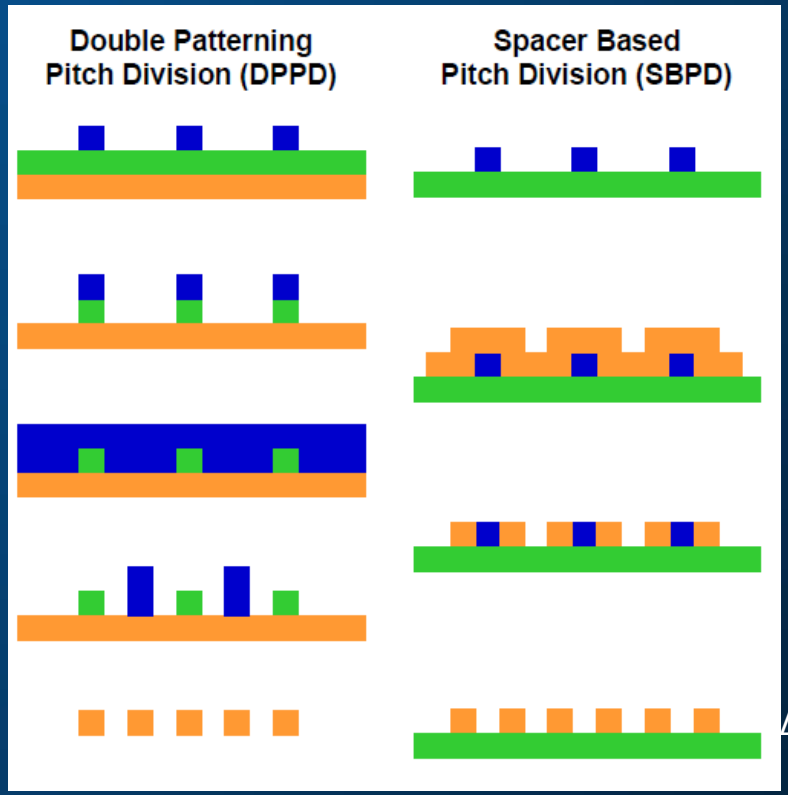
$$\frac{\text{bits}}{\text{pixel}} = \log_2\left(1 + \frac{A_p}{\Delta\text{PV}}\right). \quad (5)$$

constant

$$\frac{\text{bits}}{m^2} = \left\lceil \frac{\text{NA}}{k_1\lambda} \right\rceil^2 \log_2(M_H) = \left[\frac{\text{NA}}{k_1\lambda}\right]^2 \log_2\left(1 + \frac{A_p}{\Delta\text{PV}}\right). \quad (6)$$

ΔPV=2*EPE gets worse with more levels of Pitch Division

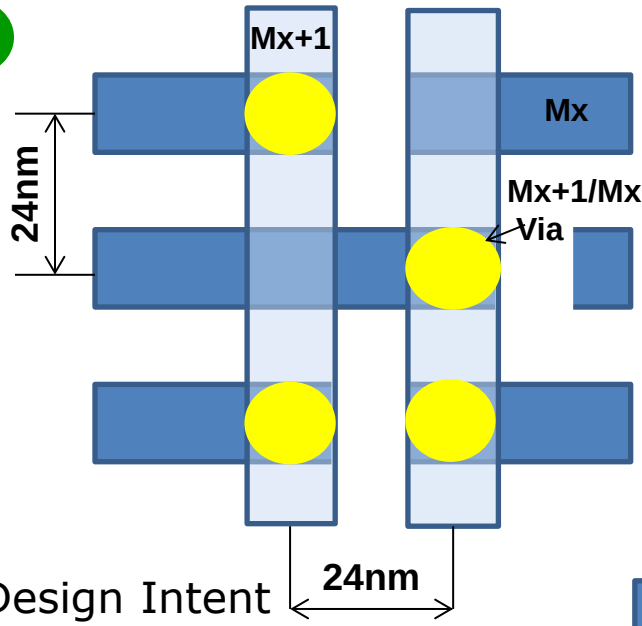
Whichever way you cut it



every nth split adds Edge Placement Error.

Process Information Transfer Capacity of Split/Divided Exposures

1



1. Design Intent

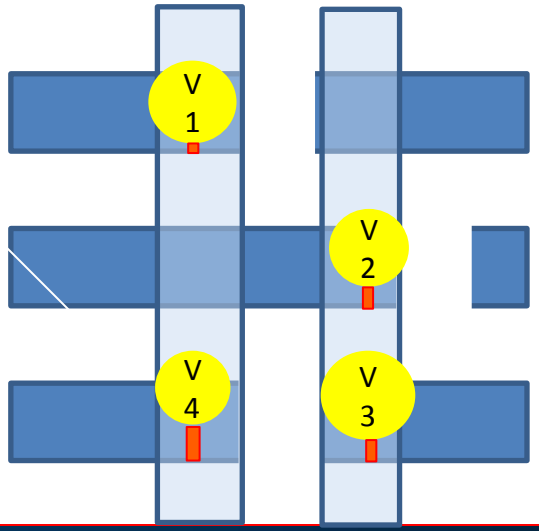
every nth split adds Edge Placement Error

2 Single Damascene

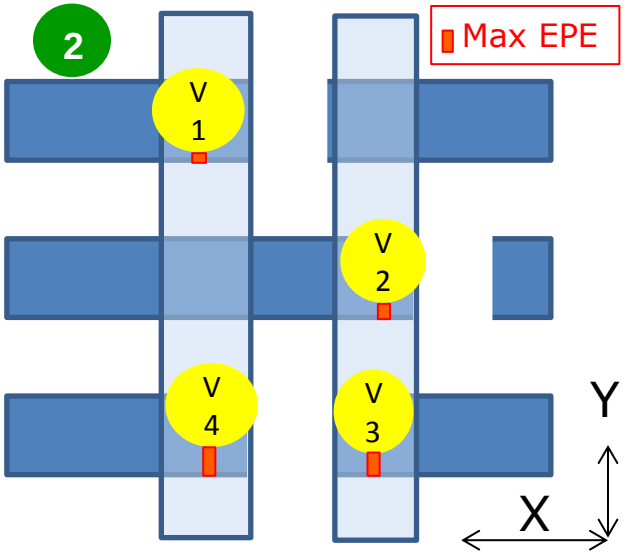
No EPE on Mx & Mx+1
No CDU EPE.
EPE only to Overlay.

V1 aligns to Mx in Y,
Mx end of line in X.

V2 aligns to V1 in X&Y
V3 to V2, V4 to V3.



2



3

Same as 2 with addition of non zero CDU to EPE

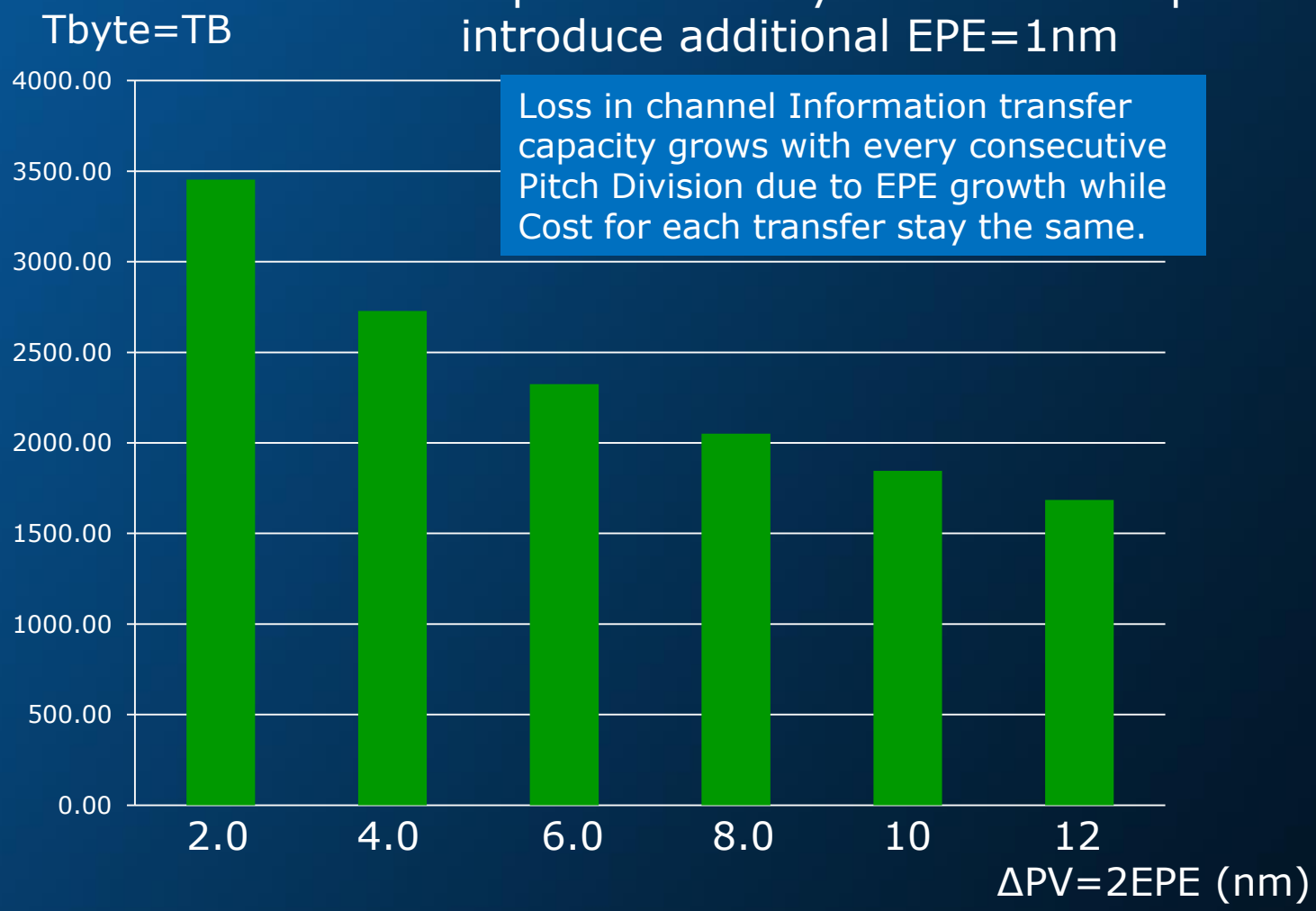
EPE accumulates with Split Exposures

Split/Divided Exposures Lithography Tooling Cost and Productivity

Information transfer capacity by exposure tool in 1 hour for $1,000 depreciated cost

193i -1.35NA
$50M/Tool
TPT=240WPH
Field 26X33mm
Depreciation 4y
ΔPV 1st =2nm

Case Study: Layer layout split in several exposures. Every consecutive exposure introduce additional EPE=1nm

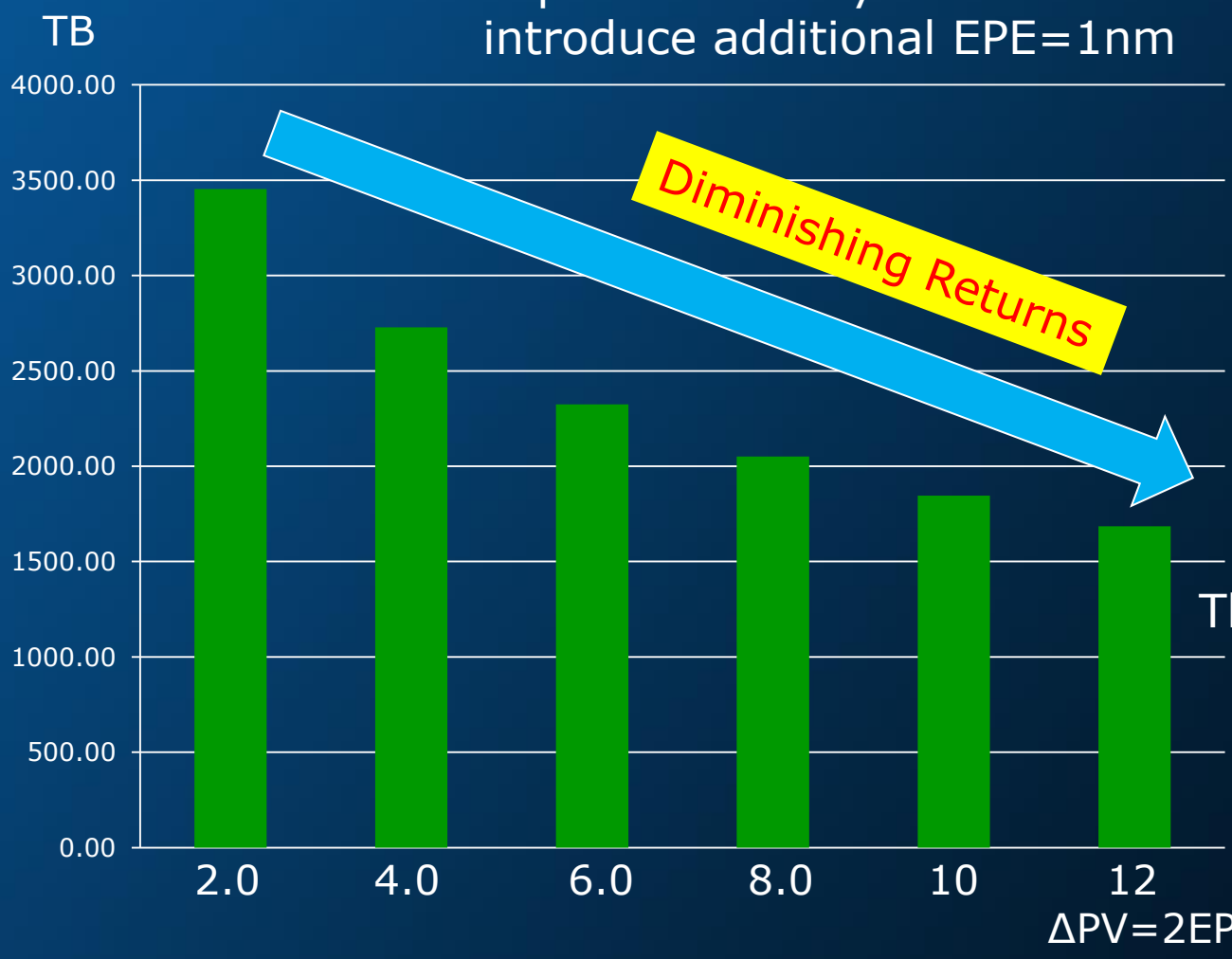


Loss in channel Information transfer capacity grows with every consecutive Pitch Division due to EPE growth while Cost for each transfer stay the same.

New Generation Lithography – Tooling Cost and Productivity

Information transfer capacity by exposure tool in 1 hour for $1,000 depreciated cost

193i -1.35NA
$50M/Tool
TPT=240WPH
Field 26X33mm
Depreciation 4y
ΔPV 1st =2nm



Case Study: Layer layout split in several exposures. Every consecutive exposure introduce additional EPE=1nm

That's why

New Generation Lithography – Manufacturing Perspective

NGL under Development:

Diffraction Limited Imaging	= EUVL
Self Organizing Materials	= DSA
Charged Particles Optics	= EBDW
Embossing	= Imprint

Manufacturing is about Cost and Yield

Cost is about Tooling/Materials Price and Productivity

Yield is about Process Control and Defects

Defect Reduction and Process Control depend on ability to "see" and measure features of interest - Metrology

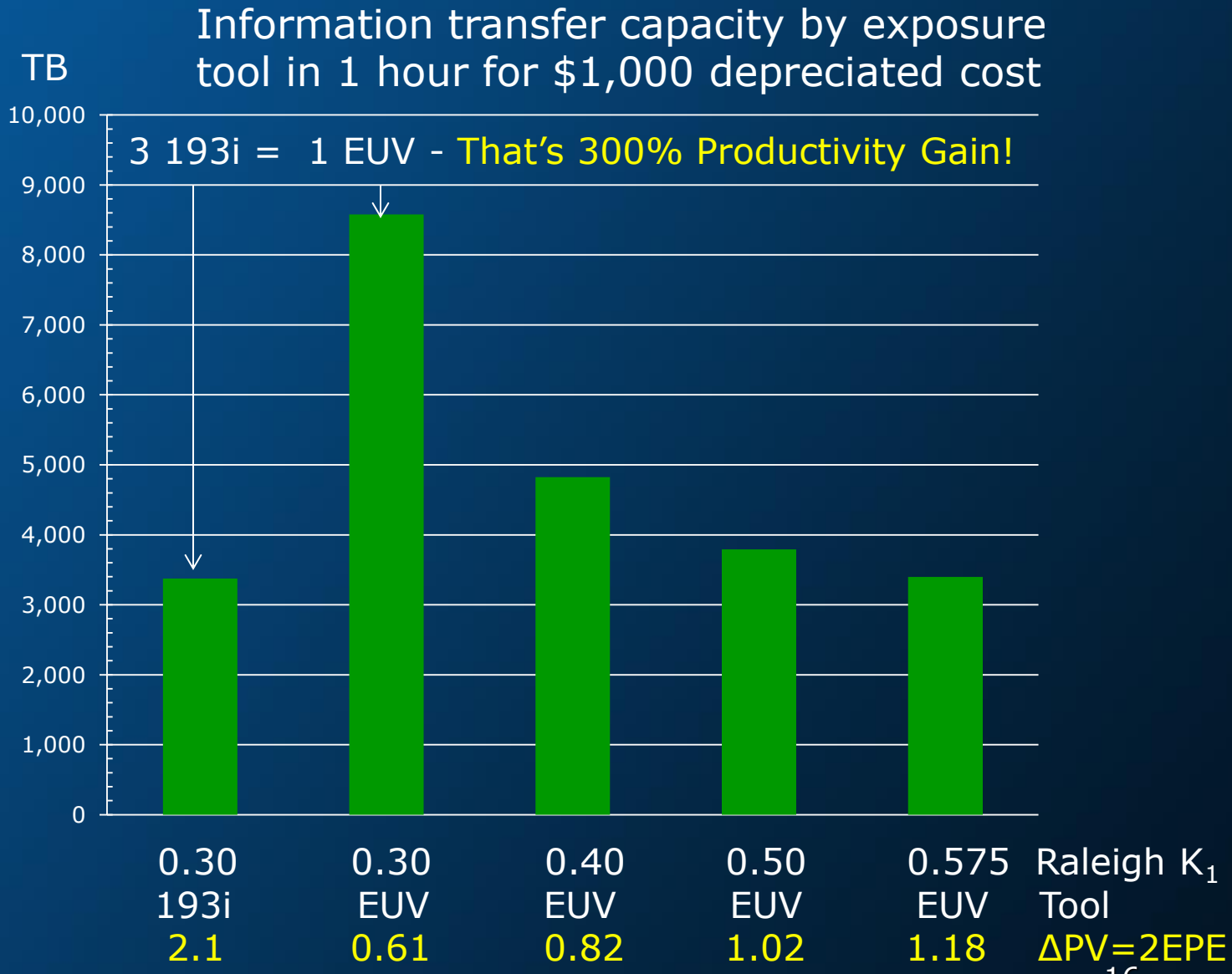
Better resolution than 193i is necessary but not sufficient!

New Generation Lithography – Information Transfer Cost and Productivity

193i -1.35NA
$50M/Tool
TPT=240WPH

EUV – 0.33NA
$100M/Tool
TPT=100WPH

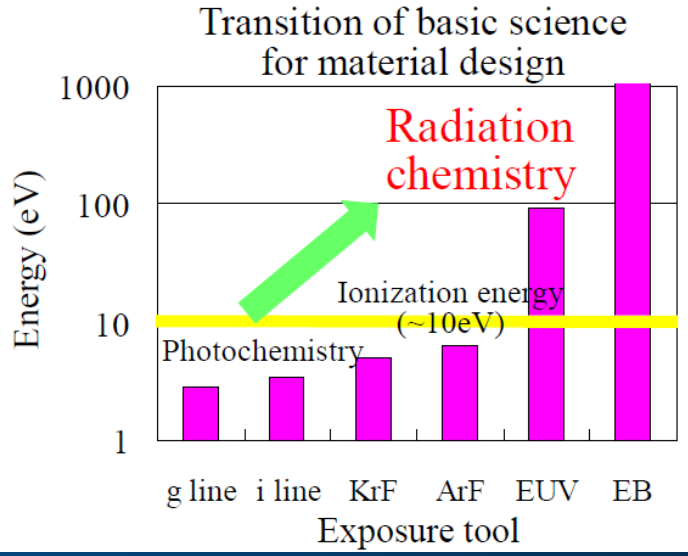
Both Tools:
Field 26X33mm
Depreciation 4y
ΔPV=0.05Ap

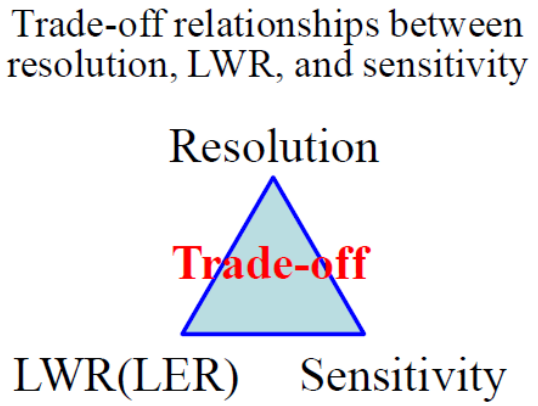


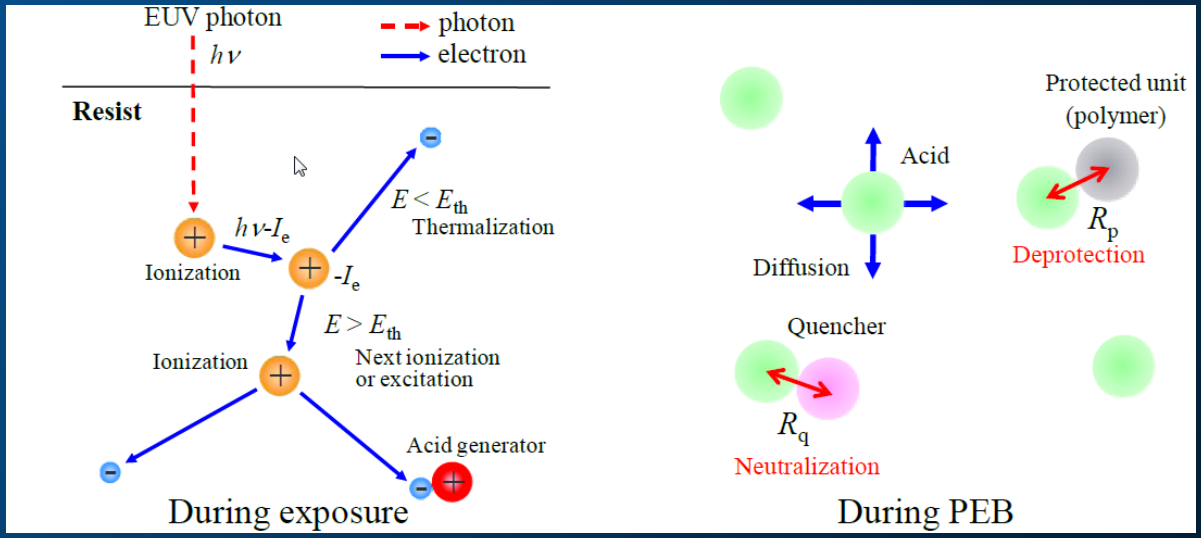
New Generation Lithography – Information Transfer Process Control

EUV and EBDW use different resist chemistry than 193nm resulting in challenging EPE Control and EPE and Productivity trade-offs

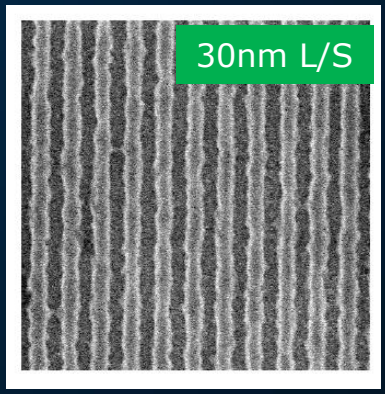
"Nanochemistry in Chemically Amplified Resists Used for Extreme Ultraviolet Lithography" Takahiro Kozawa, Osaka University, EIPBN 2013



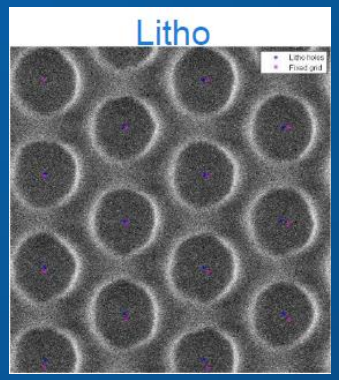


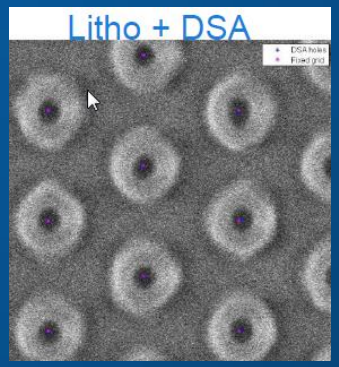


EUV 15mj/cm^2 EIDEC Resist



New Generation Lithography – Information Transfer Process Control

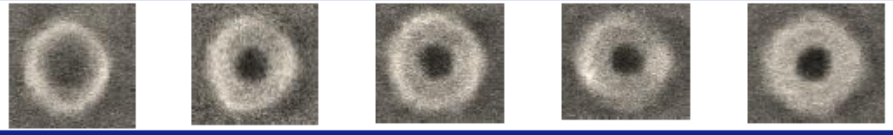




"Thermodynamic origin of placement errors for contact holes created by directed self-assembly"
Sander Wuister et al,
ASML, Phillips Research,
EIPBN 2013, Nashville, USA

ASML

Experimental results for cylindrical phase *					
Litho CD [nm]	66	72	76	79	83
DSA CD [nm]	closed	29	29	29	30
Placement error [nm]	-	2.4	2.3	2.1	2.1



Simulations for cylindrical phase					
Litho CD [nm]	66	72	76	79	83
DSA CD [nm]	closed	15	19	20	22
Placement error [nm]	-	2.1	2.2	2.1	1.9

$$3\sigma_{DSA} = 3\sqrt{\sigma^2_{litho+DSA} - \sigma^2_{litho}}$$

BCP DSA Molecular dynamic and kinetic create its own EPE Challenges and Productivity trade-offs

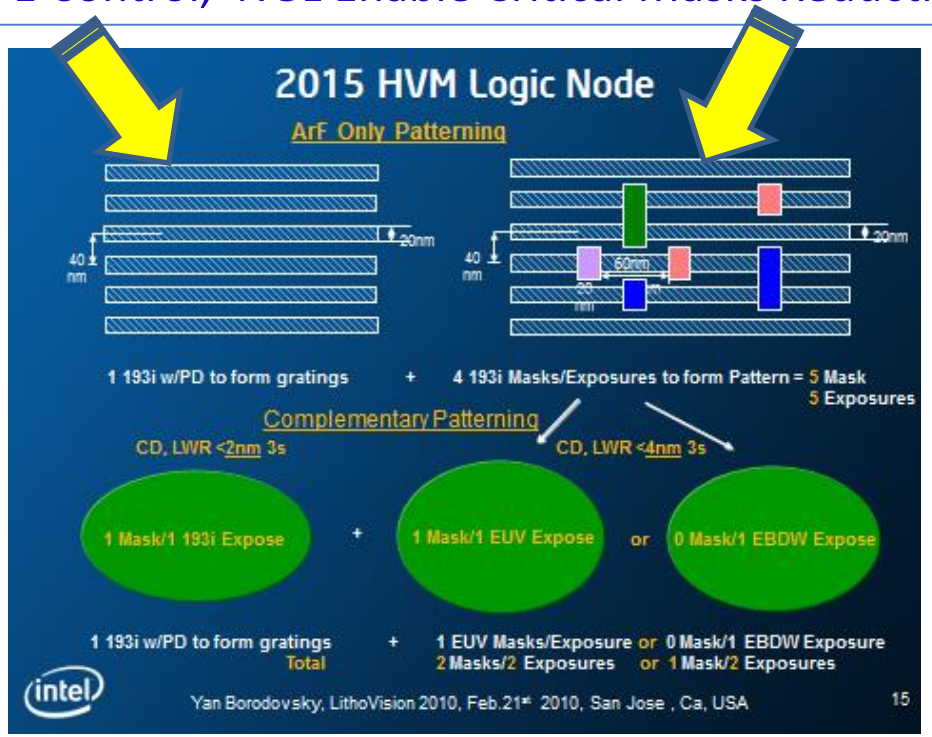
Complementary Lithography - View 2012

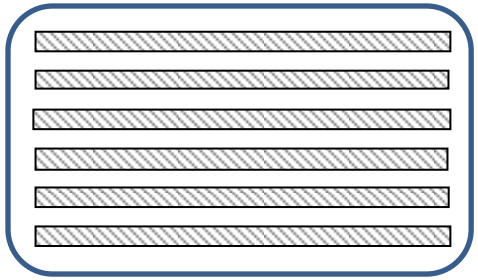
193i Gratings provide Critical EPE Control, NGL Enable Critical Masks Reduction

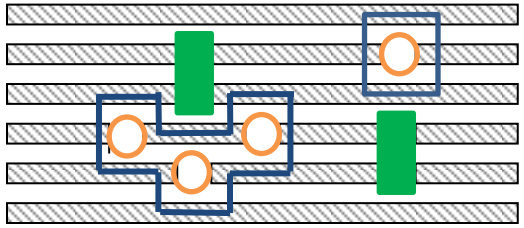
Gridded Layouts –
193i + Pitch Division
+ EUV Cuts
with HVM EUV

Gridded Layouts –
193i + Pitch Division
+ EBDW Cuts
with HVM EBDW

Gridded Layouts –
193i + Pitch Division
+ DSA Cuts
with HVM DSA



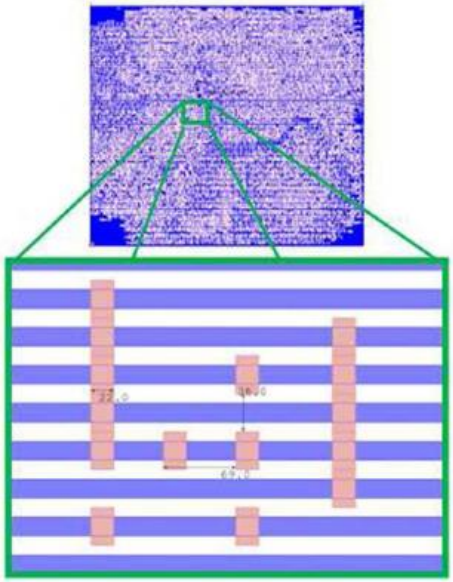




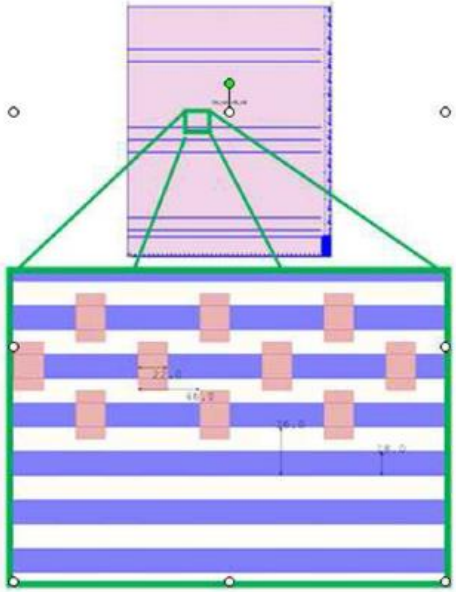
Complementary Lithography – EBDW Demonstrated at LETI/IMAGINE

18 nm hp joint work with TELA Innovation

Logic block



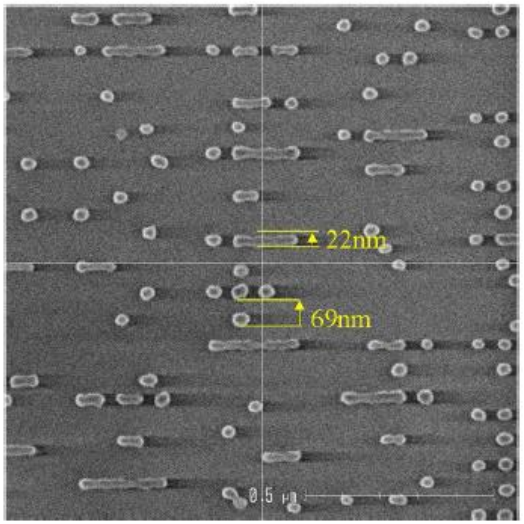
SRAM block



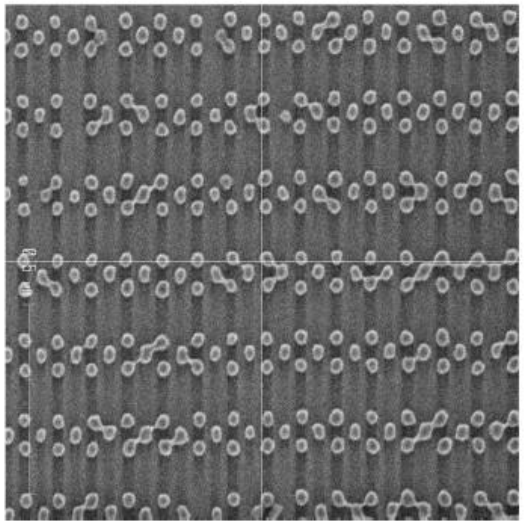
Complementary Lithography – EBDW Demonstrated at LETI/IMAGINE

18 nm hp with MAPPER platform

Logic block



SRAM block



Positive tone: 90% density

Complementary Lithography – DSA at LETI/IDeAL

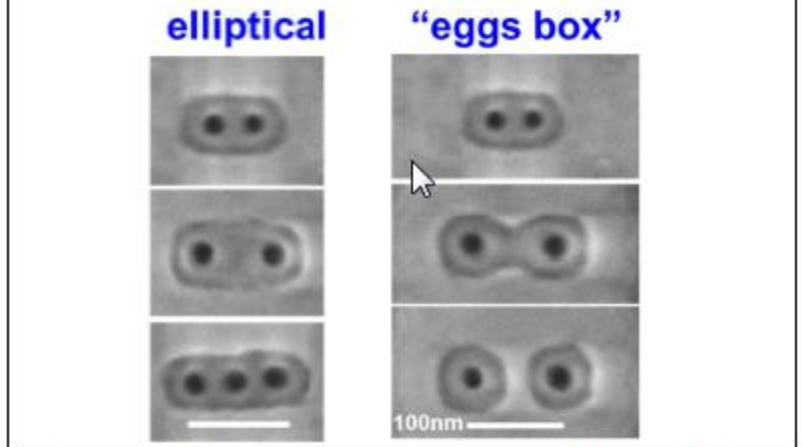


Figure 14: Contact doubling in elliptical and "eggs box" like structure using BCP;

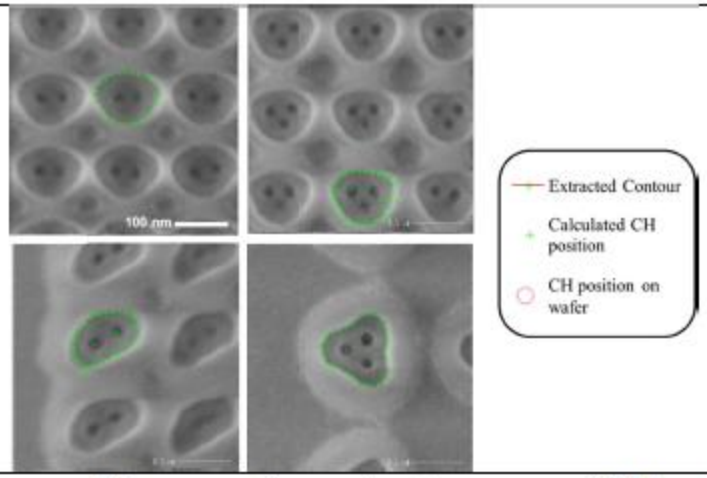


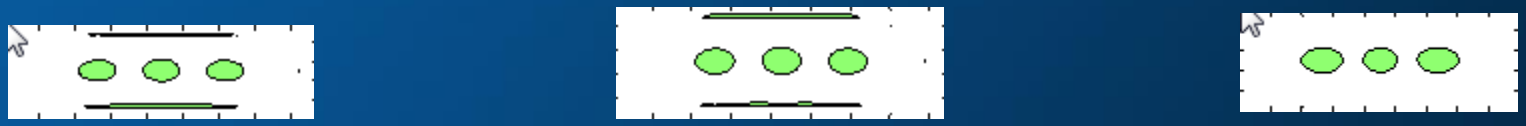
Figure 15: complex structures available for contact multiplication by DSA.

The potential of block copolymer's directed self-assembly for contact hole shrink and contact multiplication

R.Tiron et al, Proc of SPIE Volume 8660, 2013

Basic Capabilities for Cylinders Multiplications needed for Complementary Lithography Demonstrated by Leti led IDeAL

Challenges Remaining - DSA

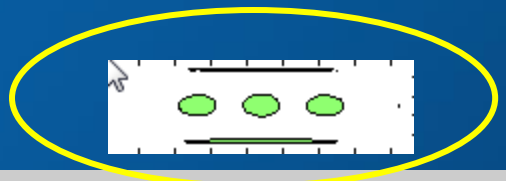


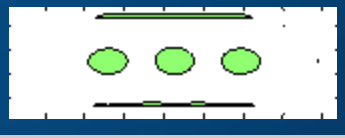
These are SCFT simulated images of top down SEM for holes produced by removing PMMA from PS matrix in 3 slightly different templates.

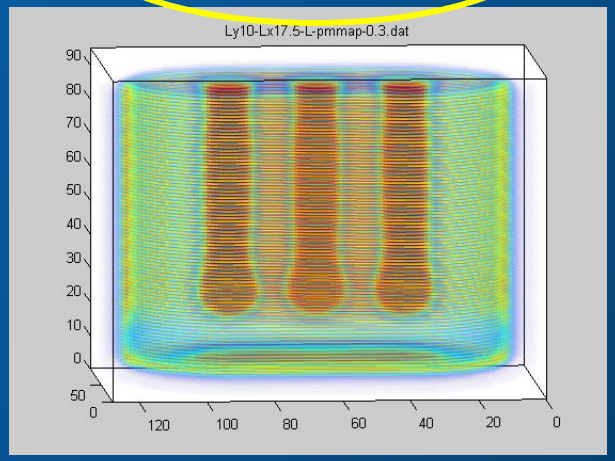
One is “good”, two are not.

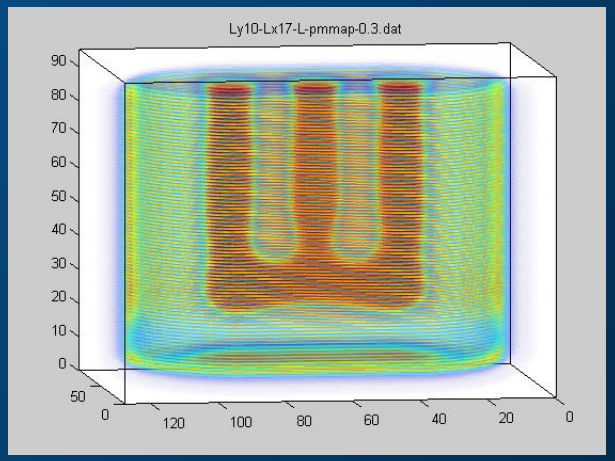
Which one is good?

Challenges Remaining- DSA



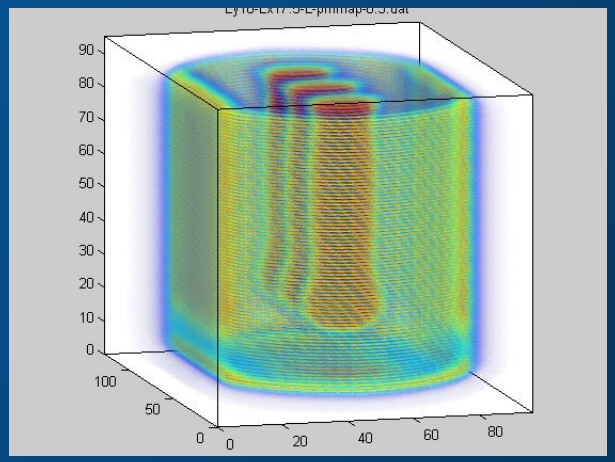


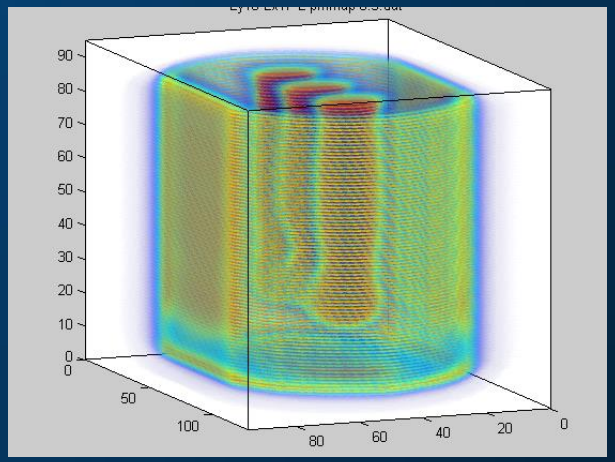


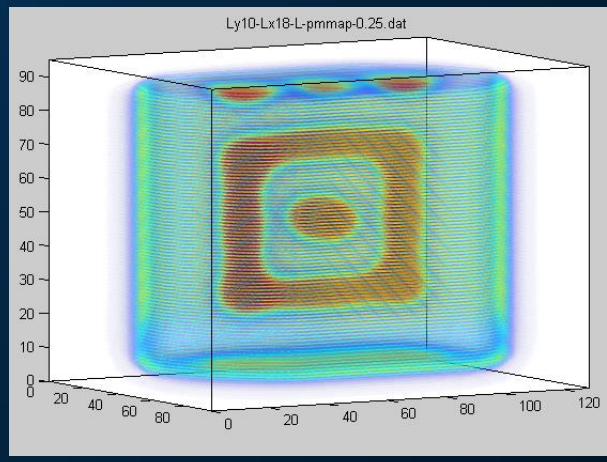


Templated DSA–3D SCFT dimensional, surface energy and composition changes reveals defects undetectable by Top Down SEM.

No Metro = No HVM



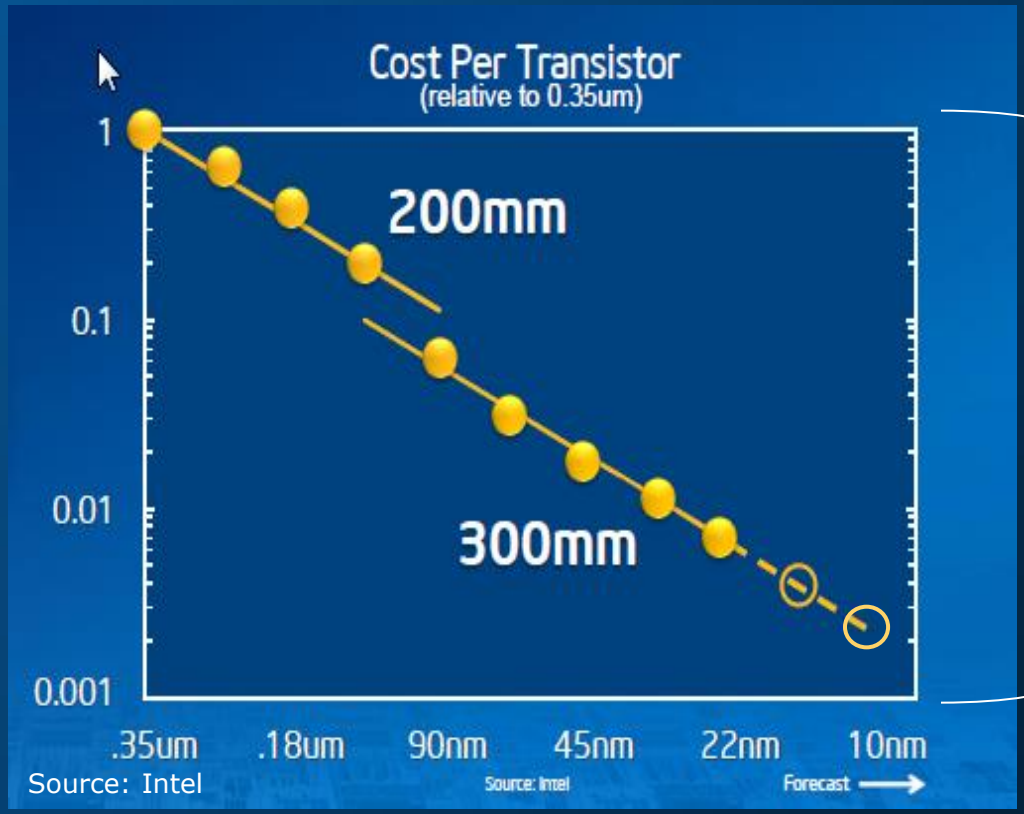




3.5nm Template Trench Length Difference.

New Generation Lithography - Yield

Diffraction Limited Imaging = EUVL
Self Organizing Materials = DSA
Charged Partices Optics = EBDW
Embossing = Imprint



Existing Paradigm

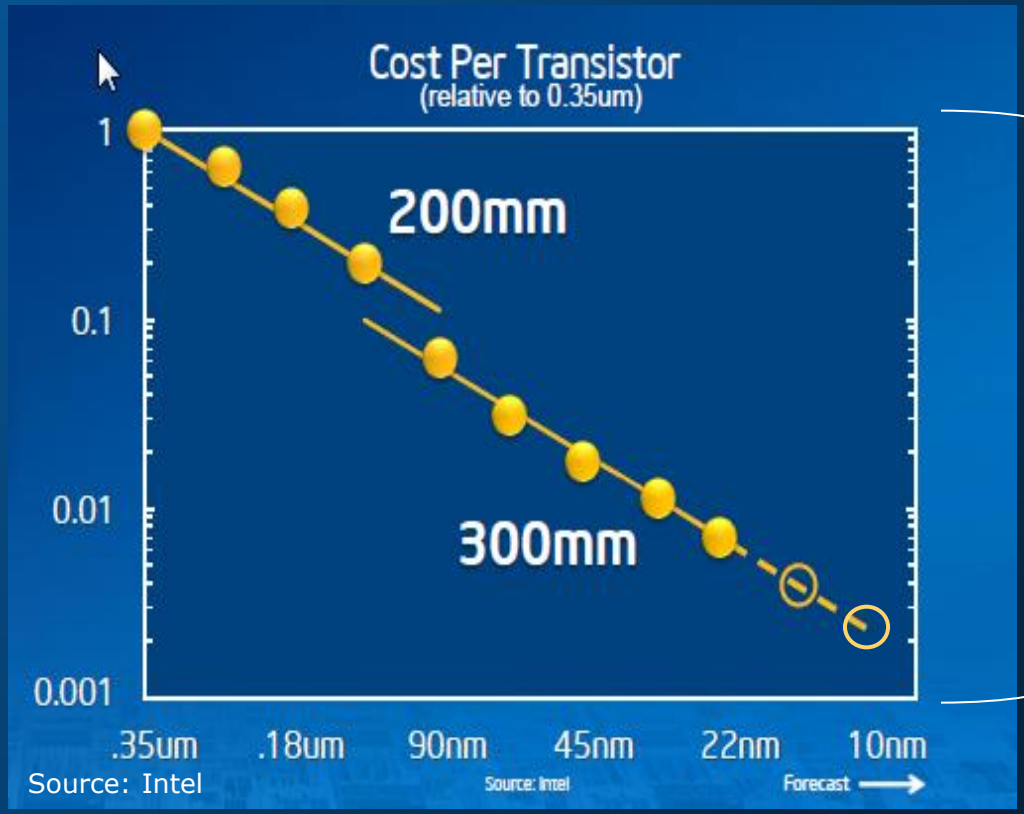
0 Defect Mask + Pellicle =

- Defect free pattern
- Low EP uncertainty

- True & tried EPE Metrology and Dispo

New Generation Lithography - Defects

Diffraction Limited Imaging = EUVL - Mask Infrastructure Develop
Self Organizing Materials = DSA - Prohibitively Large now
Charged Partices Optics = EBDW - Unknown for HVM
Embossing = Imprint - Prohibitively Large for MPU



Existing Paradigm

0 Defect Mask + Pellicle =

- Defect free pattern
- Low EP uncertainty

- True & tried EPE Metrology and Dispo

- <0.01 defect/cm2 per litho step

New Generation Lithography - Opportunity

		Defects
Diffraction Limited Imaging	= EUVL	- Mask Infrastructure Develop
Self Organizing Materials	= DSA	- Prohibitively Large now
Charged Particles Optics	= EBDW	- Unknown for HVM
Embossing	= Imprint	- Prohibitively Large for MPU

LETI's IMAGINE and IDeAL Programs are in a forefront of NGL Litho Technology Incubation and Maturation.

Basic EBDW and DSA Capabilities Demonstrated by Imagine and IDeAL in support of Complementary Lithography look promising.

Both EBDW and DSA are Maskless Technologies.

Reliable Defect Detection and Metrology is a must for introduction of maskless lithography in HVM. Focus on those will help greatly DSA and EBDW maturation.

Edge Placement Errors Control is of Critical importance to maturation of EBDW and DSA.

EPE vs Productivity trade-offs must be understood for EBDW and DSA maturation and IC Industry adoption.

Existing Paradigm

0 Defect Mask + Pellicle =

- Defect free pattern
- Low EP uncertainty

- True & tried EPE Metrology and Dispo

- <0.01 defect/cm2 per litho step

Thank you for your attention